IN THE CLAIMS:

Please cancel all pending claims, including claims 1-14.

Please add the following new claims 15-23:

15. (New) An apparatus comprising:

a instruction decoder to receive an unpack instruction;

a first register to hold a first packed data having a first plurality of packed data elements including a first packed data element and a third packed data element;

a second register to hold a second packed data having a second plurality of packed data elements including a second packed data element and a fourth packed data element;

a third register to hold a third packed data;

a circuit coupled to the decoder to receive the first packed data from the first register and the second packed data from the second register and to unpack the first packed data and the second packed data responsive to the unpack instructions by copying the first packed data element into the third register, copying the second packed data element into the third register adjacent to the first packed data element, copying the third packed data element into the third register adjacent to the second packed data element, and copying the fourth packed data element into the third register adjacent to the third packed data element.

16. (New) A digital processing apparatus comprising:

a decoder to receive an unpack control signal having an Intel integer opcode format comprising three or more bytes, a third byte of the three bytes permitting a first three-bit source register address and a second three-bit source-destination register address;

a first register to hold a first packed data having a first plurality of packed data elements including a first packed data element and a third packed data element, the first

register corresponding to the first three-bit source register address;

a second register to hold a second packed data having a second plurality of packed data elements including a second packed data element and a fourth packed data element, the second register corresponding to the second three-bit source-destination register address;

a circuit to receive the first packed data from the first register and the second packed data from the second register, and in response to the unpack control signal, to copy the first packed data element into the second register, copy the second packed data element into the second register adjacent to the first packed data element, copy the third packed data element into the second register adjacent to the second packed data element, and copy the fourth packed data element into the second register adjacent to the third packed data element.

17. (New) The digital processing apparatus recited in Claim 16 wherein the decoder is further to receive the unpack control signal having an Intel integer opcode format as described in the "Pentium® Processor Family User's Manual," the Intel integer opcode format comprising three or more bytes, a first byte and a second byte of the three bytes permitting an operation code to specify an unpack operation interleaving low order packed byte elements, word elements or doubleword elements from the first and second packed data;

18. (New) A computer system comprising:

a memory to hold an upack instruction having an Intel integer opcode format comprising three or more bytes, one of the three bytes permitting a first three-bit source register address and a second three-bit source-destination register address;

a storage device to hold software, the software configured to supply the unpack instruction to the memory for execution;

a processor enabled to receive and decode the unpack instruction from the memory, the processor including: a first register corresponding to the first three-bit source register address to hold a first packed data having a first plurality of packed data elements including a first packed data element and a third packed data element, a second register corresponding to the second three-bit source-destination register address to hold a second packed data having a second plurality of packed data elements including a second packed data element and a fourth packed data element, and a circuit to receive the first packed data from the first register and the second packed data from the second register and to copy the first packed data element into the second register, copy the second packed data element into the second register adjacent to the first packed data element, copy the third packed data element into the second register adjacent to the second packed data element, and copy the fourth packed data element into the second register adjacent to the third packed data element.

19. (New) A method comprising:

receiving an unpack instruction, said unpack instruction comprising an opcode field, a first field to indicate a first operand having a first plurality of data elements including a first data element and a second data element, and a second field to indicate a second operand having a second plurality of data elements including a third data element and a fourth data element, each of the first data element, the second data element, the third data element, and the fourth data element having a length of N/2 bits;

storing an unpacked data element having a length of N bits in response to said unpack instruction, said unpacked data element comprising the first data element but not the second data element of the first operand, and the third data element but not the fourth data element of the second operand.

20. (New) The method recited in Claim 19 wherein the first data element is a low order data element of the first operand and the third data element is a low order data element of the second operand and the opcode field of the unpack instruction contains one of a set of operation codes to specify an unpack operation interleaving low order byte elements, word elements or doubleword elements from the first and the second pluralities of data elements.

21. (New) The method recited in Claim 20 wherein the opcode field of the unpack instruction contains one of a set of operation codes comprising the hexadecimal values 0F60, 0F61 and 0F62.

22. (New) The method recited in Claim 20 wherein the first data element is a high order data element of the first operand and the third data element is a high order data element of the second operand and the opcode field of the unpack instruction contains one of a set of operation codes to specify an unpack operation interleaving high order byte elements, word elements or doubleword elements from the first and the second pluralities of data elements.

23. (New) The method recited in Claim 22 wherein the opcode field of the unpack instruction contains one of a set of operation codes comprising the hexadecimal values 0F68, 0F69 and 0F6A.